Bharati Vidyapeeths College Of Engineering For Women,Pune.

Unit Test-1
Marks-30
Time-1hr
Year:2009

Q1.Compare Moore and Mealy Model in Digital Design? [06]
Q2 Design a sequene detector to detect the following sequence using D-flipflops….110…. [06]
Q3What are the different types of VHDL modeling?Explai any one in detail? [06]
Q4 Write a VHDL code for3:8 Decoder ? [06]
Q5Explain in detail Carry Lookahead Adder? [06]

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Unit Test-11
Marks-30
Time-1hr
Year:2009

Q1. Explain the following: [08]

a) Stacks & Subroutines
b) Indexed Addressing.

Q2.What is DMA? Explain three modes of DMA operation with flow charts? [08]

Q3 Explain The Use of Bus Arbitration Method? [08]

Q4 Write short note on CD-ROM,RAID [04]

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