BHARATI VIDYAPEETH COLLEGE OF ENGINEERING FOR WOMEN ,PUNE

SE-II(E & TC) - (2010-11 SEM I)

UNIT TEST-II

SUB: DLD **MARKS:30** **TIME:1 hr**

Q.1)Design Mod -5 counter 8M

Q.2)Design and implement the following sequence generator using T-ff. 7M

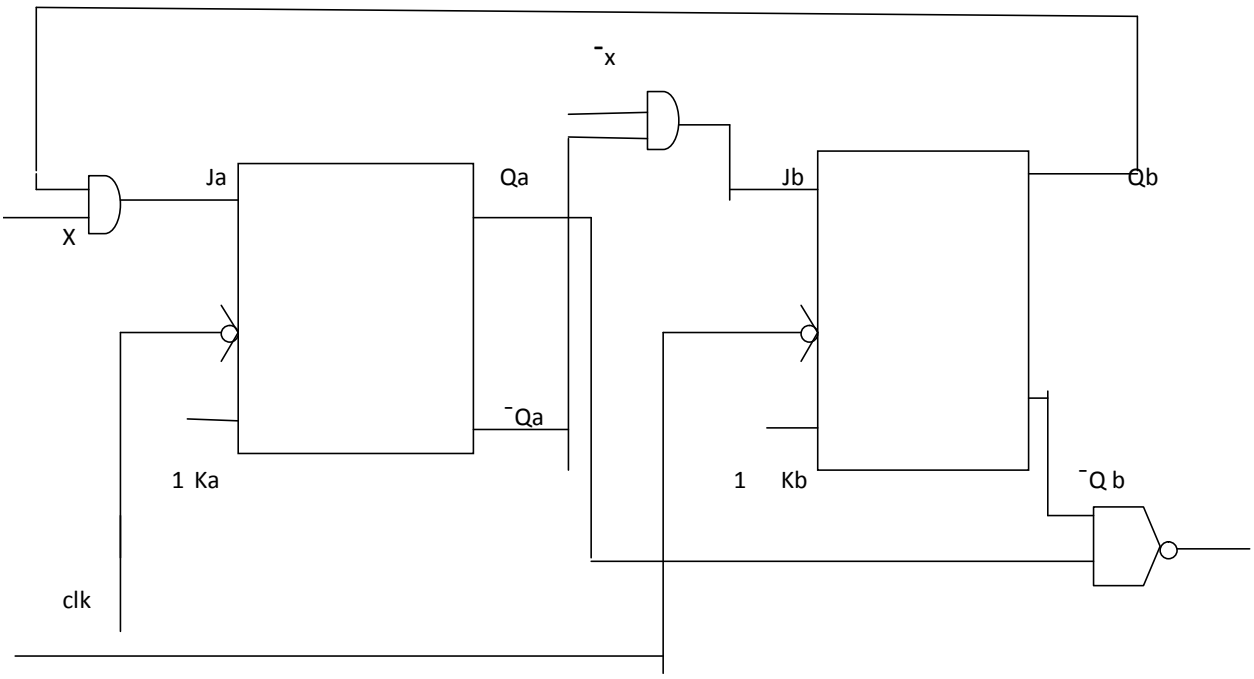
Q.3) Convert D ff to JK ff. 8M

Q.4) Design a sequence detector to detect tha following sequence using JK ff.

……1010….. 7M

Or

Q.5)Determine the following ckt write the state table n draw state diagram….7M



BHARATI VIDYAPEETH COLLEGE OF ENGINEERING FOR WOMEN, PUNE

SE-II (E & TC) - (2010-11 SEM I)

UNIT TEST-I

SUB: DLD **MARKS:30** **TIME:1 hr**

Q.1)A) Simplify the following function using Quine Mccluskey method

F(a,b,c,d)=∑m(0,1,2,3,5,7,8,9,11,14) 10M

B)Design two bit comparator using logic gates. 5M

or

Q.1) A)Brifely explain operation of look ahead carry generator 6M

B)Design and implement following function using 4:1 Mux with active low strobe Input f(a,b,c,d)= ∑m(2,3,5,7,8,9,12,13,14,15) 9M

Q.2) Design and implement Mod-24 ripple counter using IC7490 7M

B)Give the different type of Shift register also draw the diagram of 3 bit bidirectional Shift register 8M

Or

Q.2)A)Convert JK ff into Dff and T ff and also design and implement 4 bit Johnson Counter 8M

B) Design and implement Mod-10 ripple counter using JK ff and explain With outut waveforms. 7M

Bharati Vidyapeeth's College of Engineering for Women, Pune

Electronics and Telecommunication Department

Unit Test:1 (Marks:30) Academic Year:2010-11

Subject: Digital Logic Design

Q.1a) Minimise the function by using 8:1 Mux.
f(a,b,c,d)=∑ m(0,1,3,4,5,7,9,11,15).....6 M

Q.1b) Design 16:1 Mux by using 8:1 Mux..?.....4 M

Or

Q.1a)Implement the full Adder by using Multiplexer?.....6 M

Q.1b) What is bcd to seven segment decoder?,.....4 M

Q.2a) Draw waveforms for JK F/F and draw its timing diagram?.....6 M

Q.2b) Design and Implement MOD 25 asynchronus counter and Mod 6 down counter by using appropriate IC?.....10 M

Or

Q.2b) Design and implement 4 bit up synchronous counter.....10 M

Q.3) What do you mean by register give the types of registers?.....?.....4 M

Bharati Vidyapeeth's College of Engineering for Women, Pune

Electronics and Telecommunication Department

Unit Test:1 (Marks:30) Academic Year:2008-09

Subject: Digital Logic Design

Q.1a) Minimise the function by using K-Map and implement by using only NAND gates. $f(a,b,c,d)=\pi\ m(0,1,3,4,5,7,9)$.....6 M

Q.1b) Design full adder by using two half adder?.....4 M

Or

Q.1a)Implement the full Adder by using Multiplexer?.....6 M

Q.1b) What is Gray code? Convert one binary no into gray code.....4 M

Q.2a) Convert JK F/F into T and D F/F.....6 M

Q.2b) Design and Implement 3 bit up down ripple counter?.....10 M

Or

Q.2b) Design and implement 3 bit up synchronous counter.....10 M

Q.3) What do you mean by latch ? What do you mean by Flip Flop?.....4 M

Bharati Vidyapeeth's College of Engineering for Women, Pune

Electronics and Telecommunication Department

Unit Test:1 (Marks:30) Academic Year:2009-10

Subject: Digital Logic Design

Q.1a) Minimise the function by using K-Map and implement by using only NOR gates.
$f(a,b,c,d)=\sum m(0,1,3,4,5,7,9) +d(2,8)$.....6 M

Q.1b) Design full adder by using two half adder?.....4 M

Or

Q.1a)Implement the full subtractor by using Multiplexer?.....6 M

Q.1b) Design 8:1 mux by using 4:1 Mux?.....4 M

Q.2a) Convert SR F/F into T and D F/F.....6 M

Q.2b) Design and Implement BCD to seven segment decoder?.....10 M

Or

Q.2b) Design and implement 3 bit up/down ripple counter.....10 M

Q.3) What do you mean by latch ? What do you mean by Flip Flop?.....4 M

Bharati Vidyapeeth's College of Engineering for Women, Pune

Electronics and Telecommunication Department

Unit Test:II (Marks:30) Academic Year:2010-11

Subject: Digital Logic Design

Q.1a) Write a short note on flow of VHDL.....6 M

Q.1b) Write a program for 4 bit up/down ripple counter?.....6 M

Or

Q.1a)What is the difference between moore and mealy machine?.....6 M

Q.1b) Write a VHDL code for 4 bit synchronous up counter..?.....,.....6 M

Q.2a) Write a short note on totam pole?.....6 M

Q.2b) Write short note on digital logic families?.....8 M

Or

Q.2b) Write short note on TTL and CMOS interfacing.....8 M

Q.3) Draw the diagram of two input nand gate by using NMOS..... 4 M

Bharati Vidyapeeth's College of Engineering for Women, Pune

Electronics and Telecommunication Department

Unit Test:II (Marks:30) Academic Year:2008-09

Subject: Digital Logic Design

Q.1a) Write a short note on VHDL.....6 M

Q.1b) Write a program for full adder by using two half adders by using structural method?.....6 M

Or

Q.1a)What are the different types of Modelling styles write a short note?.....6 M

Q.1b) Write a VHDL code for 8:1 Mux?.....,.....6 M

Q.2a) Write a short note on State machines?.....6 M

Q.2b)Using D F/F design synchronous counter that has the following sequences?

0-2-5-6-0 .....8 M

Or

Q.2b) Design and implement sequence detector for 1101 sequence by using moore machine? .....8 M

Q.3) Draw the diagram of two input nor gate by using NMOS..... 4 M

Bharati Vidyapeeth's College of Engineering for Women, Pune

Electronics and Telecommunication Department

Unit Test:II (Marks:30) Academic Year:2009-10

Subject: Digital Logic Design

Q.1a) Write a short note on VHDL Modelling styles?.....6 M

Q.1b) Write a VHDL program for 2 bit comparator?.....6 M

Or

Q.1a)What are the advantages of VHDL on Conventional method?.....6 M

Q.1b) Write a VHDL code for 4 bit ALU?.....,.....6 M

Q.2a) Write a short note on ASM and FSM?.....6 M

Q.2b)Using T F/F design synchronous counter that has the following sequences?

0-1-4-6-0 .....8 M

Or

Q.2b) Design and implement sequence detector for 1101 sequence by using mealy machine? .....8 M

Q.3) Draw the diagram of two input nand gate by using PMOS..... 4 M