BHARATI VIDYAPEETH'S COLLEGE OF ENGG. FOR WOMEN

UNIT TEST-I (2010-11)

CLASS:- BE(E & TC) SUB:- VLSI DESIGN MARKS:-30

Q1. Differentiate function and procedure. what do you mean by subprogram overloading.(9)

OR

Q1. Write VHDL codes for 8:1mux using 2:1 mux with structural modeling .(9)

Q2. Explain any two attributes in detail.(6)

Q3. What do you mean by metastability? what are the solutions? explain any one solution in detail (9)

OR

Q3. Compare various encoding techniques. which is most suitable foe FPGA? why?(9)

Q4. Differentiate synchronous asynchronous machine.(6)

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UNIT TEST-I (2009-10)

CLASS:- BE(E & TC) SUB:- VLSI DESIGN MARKS:-30

Q1] Explain VLSI design flow in detail with respect to EDA tool.(9)

Q2] Write VHDL code for 4 bit shift register for SISO operation.(9)

OR

Q3] Draw the state diagrm and write VHDL code for traffic light controller(9)

Q3] Explain in brief: delta delay(4)

Q4] What is metastability?How to avoid it?(8)

OR

Q5] Differentiate between: (8)

a)Function and procedure

b)Signal and variable

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UNIT TEST-I (2011-12)

CLASS:- BE(E & TC) SUB:- VLSI DESIGN MARKS:-30

Q.1) Explain design flow in detail.mention the tools used st each step.(5)

Q.2) What are the different modeling styles of architecture.how to make a decision?(5)

Q.3) What is metastability?(4)

Q.4) Draw the FSM and write VHDL code for J-k flip flop.(6)

Q.5) Write VHDL code for 8 bit shift register.(5)

Q.6) Explain the basic architecture of CPLD?(5)

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UNIT TEST-II (2009-10)

CLASS:- BE(E & TC) SUB:- VLSI DESIGN MARKS:-30

Q1] Explain boundary scan in detail,what is BIST?(8)

Q2] Explain JTAG.What are the various pins involved?(8)

Q3] With suitable schematic explain stuck-at faults.What is meant by fault coverage?(9)

Q4] Why is DFT needed and explain in brief with suitable example.(9)

Q5] What is technology scaling?What are the effects of it?(8)

Q6] Design 4:1 mux using transmission gates and compare schematic with conventional design?(8)

BHARATI VIDYAPEETH'S COLLEGE OF ENGG. FOR WOMEN

UNIT TEST-II (2011-12)

CLASS:- BE(E & TC) SUB:- VLSI DESIGN MARKS:-50

Q1] a)Explain CMOS-OPAMP in detail,brief the concepts of ctive load,current mirror,constant current source,output stage etc.give supporting expressions.(10)

b)What are the technologies to improve Rout of current sink/source?Explain cascade current source in detail(8)

Q2] a)What I sthe need of transmission gate .Explain TG in detail.Design a circuit 4:1 mux using TG.(8)

b)derive the expression for static an ddynamic powerdissipation ,compare them.(6)

c)Why is device sizising so important? Prove p=2.5Wr.(6)

Q3] a) Write short note on (8)

i)Threshold voltage

ii)Hot electron effect

iii)Channel length modulation

iv)Noise margin

b)Explore stuck at open and stuck at short in detail.(4)

BHARATI VIDYAPEETH'S COLLEGE OF ENGG. FOR WOMEN

UNIT TEST-II (2010-11)

CLASS:- BE(E & TC) SUB:- VLSI DESIGN MARKS:-30

Q1. With suitable schematic explain Anti-fuse, Sram, And Flash Technologies for PLD (9)

OR

Q1. Differentiate CPLD, FPGA, ASIC (9)

Q2.What is selection criteria of CPLD/FPGA in the system (6)

Q3. What do you understand by global clock, system clock and local clock/ what is significance of each (9)

OR

Q3.Explain the architecture of DRAM cell (9).

Q4. Explain DRC And SRC (6)